Mitigation of inrush and outrush currents in capacitor bank switching using dry type air core reactors

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SUMMARY

Shunt capacitor banks are extensively used in power systems for power factor correction, voltage control, power loss reduction, and power transmission capability improvement. Air core dry type reactors are often connected in series with capacitor banks in order to limit harmonic currents within the capacitors, and protect capacitor bank circuit breakers from high magnitude and rate of rise of the transient currents found in back to back switching. Outrush reactors are also used to protect nearby circuit breakers from the outrush current from capacitor banks if the nearby breaker closes into a fault. Air core reactors in applications for shunt capacitor banks are often referred to as "capacitor reactor", "inrush/outrush reactor", "transient limiting inductor (TLI)", "damping reactor", or "detuning reactors'.

This paper provides guidance in the proper selection and sizing of inrush and outrush current limiting reactors. The analytical calculations are compared with electromagnetic transient simulation results for validation.

KEYWORDS

Air core dry type reactors, Shunt capacitor banks, Inrush current, Outrush current, Circuit breaker, Capacitor reactors, Inrush current limiting reactors, Outrush current limiting reactors, Transient limiting inductors, Damping reactor, Detuning reactor, Back to back switching.

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1. INTRODUCTION

1.1. Applications of shunt capacitor banks

Shunt connected capacitor banks are widely used in transmission and distribution systems for power factor correction, voltage control, increasing the voltage stability, improving the power quality, reducing the losses, and increasing the power transmission capability of the lines.

1.2. Technical challenges

1.2.1 Harmonic current absorption

A shunt capacitor connected to a grid provides a low impedance path for higher frequency harmonic currents and thus draws harmonic currents with relatively high magnitudes which may cause vibrations and dielectric and mechanical stresses to the capacitor [1]. Addition of a series inductance increases the circuit's impedance at higher frequencies and thus avoids absorption of these currents.

1.2.2 Resonance with system

Harmonic resonance occurs when the resonance frequency of the capacitor bank and the network's equivalent reactance at the connection point matches the frequency of an existing harmonic in the system. The harmonic resonance can result in frequent tripping of capacitor banks and damage to substation equipment [2]. A cost effective and highly efficient solution is to "detune" the capacitor bank by deployment of a small series inductance to the capacitor bank.

1.2.3 Back to back switching inrush current

Capacitor banks are often connected to the bus through circuit breakers not only for protection purposes but also for frequent switching of the banks to control the bus voltage. When a bank is switched on, the other banks that are already energized will inject a current with high magnitude and frequency known as "inrush current" (see Figure 1). High di/dt of inrush current significantly increases the probability of prestrikes in closing contacts of the circuit breaker [3, 4]. The resulting prestrikes can severely damage the breaker

Figure 1. Back to back switching inrush current through circuit breaker.

contacts over time. The high di/dt value can also affect the instrumentation and control circuits, e.g. current transformers. Inrush reactors are added to reduce di/dt and peak of the inrush current.
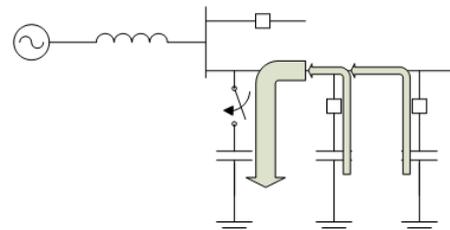
1.2.4 Outrush current

Outrush current can be defined as a high frequency, high magnitude transient current generated by an energized capacitor bank when a breaker in the neighborhood of the bank closes on to a fault (see Figure 2). An example of this situation is a reclosing breaker near a capacitor bank, with an unsuccessful reclosing attempt [5]. Outrush reactors are used to limit the outrush current.
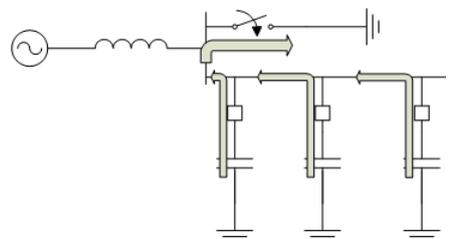

Figure 2. Outrush current flowing through a nearby circuit breaker, closing on to a fault.

1.2.5 Mitigation method

Dry type air-core reactors are widely used as a reliable, cost effective, and maintenance free solution to overcome the above technical issues in the application of shunt capacitor banks. This paper refers to relevant standards and derives the formulae to calculate the required inductances. It also provides the

formulae to determine the current ratings of these reactors including continuous, thermal short circuit, and mechanical peak currents. The accuracy of the formulae is verified by modeling the switching of three shunt capacitor banks using the transient simulation program of PSCAD.

Figure 3. Examples of shunt capacitor discharge reactor installations.

2. SWITCHING DEVICE REQUIREMENTS BASED ON STANDARDS

Important note: IEC and IEEE committees are developing standards and guides which are constantly updated. It is important to acquire the most recent relevant guidelines. Furthermore, due to continuous technical advances in circuit breakers and circuit switchers, it is important to obtain the equipment manufacturer advice on the transient current capabilities of the switching device. Generally, there are three parameters mentioned in IEC [6] and IEEE [7] standards for circuit breakers current making. These are magnitude (I), frequency (f), and their product (I×f: rate of rise of the transient current).

2.1 IEC 62271-100 [6]

This standard has the same requirement for all voltage class breakers: Inrush making current (I) $\leq$ 20 kA peak, and frequency of inrush current (f) $\leq$ 4.25 kHz [6]. IEC [6] does not specify any I×f requirement. These requirements apply to both general purpose (C0) and definite purpose (C1/C2) circuit breakers. IEC allows 130% tolerance on frequency of the inrush current for C1/C2 breakers.

2.2 IEEE C37.06 [7]

This standard has different requirements for C0 and C1/C2 breakers. In the case of C0 breakers, the requirement is I×f $< 2 \times 10^7$ and peak current smaller than the lesser of 50 kA or 1.41 times the rated short circuit current. These values are not applicable for back to back switching (refer to section 7.4, note (1) of [7]). For C1/C2 breakers, Table I applies. According to note (3) of section 7.4 in [7], the maximum frequency only applies at maximum peak current. In other words, the frequency limit can be safely violated providing the I×f requirement is met.

Table I. IEEE C37.06-2009 [7] C1/C2 switching device preferred ratings for capacitor inrush making current

Voltage class(kV)	f (kHz)	I (kA)	I×f
15.5, 25.8, 38	4.2	20	8.4×10^7
48.3	6.8	20	13.6×10^7
72.5	3.4	25	8.5×10^7
123, 145	4.3	16	6.88×10^7
170, 245	4.3	20	8.6×10^7
362, 550, 800	4.3	25	10.75×10^7

3. SINGLE CAPACITOR BANK SWITCHING
3.2 Inrush current

The maximum current magnitude (I_{peak}) and the frequency (f) of the inrush current through the circuit breaker when closing the contacts can be simply found from (1) and (2) respectively.

$$I_{peak} = \sqrt{\frac{2}{3}} \times V_{LL} \times \sqrt{\frac{C}{L_{sys}}} \qquad (1)$$

$$f = \frac{1}{2\pi\sqrt{L_{sys}C}} \qquad (2)$$

In most cases, the system impedance is large enough to limit "I", "f", and "I×f" below the standard limits. Please note that the bus and capacitor bank inductances are much smaller than that of the system and therefore are ignored in the above calculations.

3.3 Outrush current

The outrush current generated by the energized capacitor passes through a nearby circuit breaker closing on to a fault. This current has magnitude and frequency as calculated below:

$$I_{peak} = \sqrt{\frac{2}{3}} \times V_{LL} \times \sqrt{\frac{C}{L_{cap+bus}}} \qquad (3)$$

$$f = \frac{1}{2\pi\sqrt{L_{cap+bus}C}} \qquad (4)$$

Both magnitude and frequency of the outrush current mainly depend on the stray inductances of the bus and the capacitor bank. This collective inductance is typically very low and thus the outrush current has high magnitude and frequency. To limit the outrush current, a reactor is added to the bank as shown in Figure 6. With the addition of the outrush reactor and ignoring the small bus and capacitance stray inductances, "I", "f", and "I×f" values can be calculated as below:

$$I_{peak} = \sqrt{\frac{2}{3}} \times V_{LL} \times \sqrt{\frac{C}{L_{out}}} \qquad (5)$$

$$f = \frac{1}{2\pi\sqrt{L_{out}C}} \quad (6); \qquad I \times f = \sqrt{\frac{2}{3}} \times V_{LL} \times \frac{1}{2\pi L_{out}} \quad (7)$$

The required outrush inductance to limit above parameters below the standard limits is calculated in (11):

- "I×f" requirement: $L_{out} = \frac{V_{LL}}{\sqrt{6}\,\pi\,I\times f}$ (8)

  ,where "I×f" is found from section 2.2 for IEEE.

- "I" requirement: $L_{out} = \frac{2}{3}\,C\,\left(\frac{V_{LL}}{I_{peak}}\right)^2$ (9)

  ,where I_{peak} is found from section 2.2 for IEEE or section 2.1 for IEC.

- "f" requirement: $L_{out} = \frac{1}{4\pi^2 f^2 C}$ (10)

  ,where f is found from section 2.1 for IEC.

  Required L_{out}=MAX {(8), (9)} for IEEE and Max {(9), (10)} for IEC   (11)

3.4 Outrush reactor current ratings

The equipment specification provided to the manufacturer should include the outrush peak current and frequency, the thermal short circuit current and duration, and the continuous current rating, in addition to other technical parameters such as inductance, BIL, etc.

3.4.1 Continuous current rating

The rated capacitor bank current can be easily calculated as (12). This current is then multiplied by a Factor determined by the standard to include harmonic distortion (F_{hI}), capacitance tolerances (F_t), and the system overvoltage (F_v), for both grounded and ungrounded bank configurations.
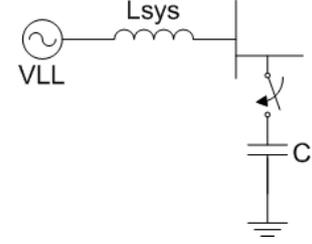

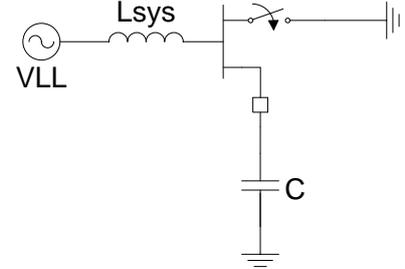Figure 4. Switching a capacitor bank.

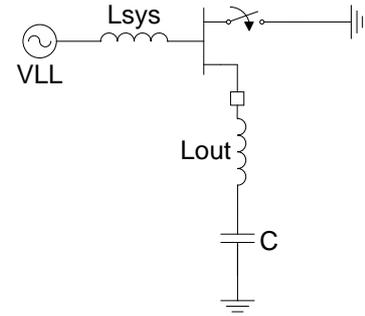

Figure 5. Outrush current from a single capacitor bank.

Figure 6. Outrush current from a single capacitor bank with reactor.

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$$I_{cap} = 2\pi f_{sys} C V_{cap,L-N} \qquad (12) \qquad\qquad I_{L_{out}} = I_{cap} \times Factor \qquad (13)$$
$$; where\ Factor = F_t \times F_{hI} \times F_v$$

Table II. IEEE C57.16-2011 [8] defined factors for continuous current rating of shunt capacitor reactors.

	Grounded bank	*Ungrounded bank*
F_t	1.1	1.1
F_{hI}	1.18	1.075
F_v	1.05	1.05
Factor	1.36	1.24

3.4.2 Short time current rating

Figure 7 shows two possible locations of a fault involving the outrush reactor. In case of Fault 1, the only current passing through the reactor is the high frequency discharge current from the capacitor bank. The peak and frequency of this current can be calculated from (5) and (6) respectively.

In case of Fault 2, the reactor will be in the path of the short circuit from the system. The DC component, and thus the peak current, of this short circuit current is maximum when the fault occurs near voltage zero crossing instant.

The reactor should be rated for thermal short circuit as in (14), and the mechanical peak current of the maximum current of the two fault scenarios explained above as in (15).
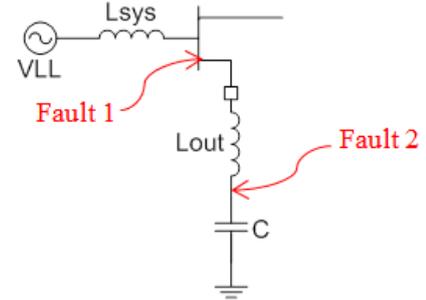

Figure 7. Fault scenarios affecting the outrush reactor of a capacitor bank.

Short circuit thermal rating: $I_{SC,rms} = \dfrac{V_{LL}}{\sqrt{3}\times 2\pi f_{sys}(L_{sys}+L_{out})}$ (14)

Mechanical peak current rating: $I_{L_{out,peak}} = \max\left\{\sqrt{\dfrac{2}{3}}\times\sqrt{\dfrac{C}{L_{out}}}\times V_{LL}\ ,\ 2\sqrt{2}I_{SC,rms}\right\}$ (15)

4. MULTIPLE CAPACITOR BANKS SWITCHING

As described in the introduction section, back to back switching of multiple capacitor banks will generate a discharge current with high magnitude and frequency. Inrush reactors are added in series with each bank to limit this inrush current. An outrush reactor is connected between the capacitor banks bus and the main bus to limit the outrush current during a close-on-to-fault event.

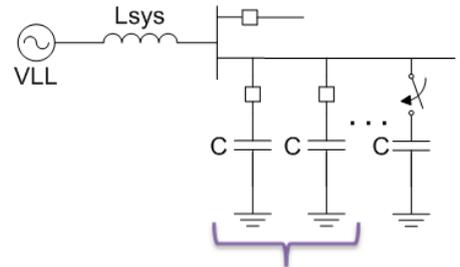### 4.1 Back to back switching inrush current

Assume "n+1" identical capacitor banks, where "n" banks are already energized and the "n+1"th bank is to be switched on, as shown in Figure 8.

When the bank "n+1" is connected at peak of the voltage, the magnitude and frequency of the inrush current from "n" banks can be found from (16) and (17), respectively.

n already energized capacitors
Figure 8. Back to back switching of capacitor banks

$$I_{peak} = \sqrt{\frac{2}{3}}\times V_{LL}\times\frac{n}{n+1}\times\sqrt{\frac{C}{L_{cap}}} \qquad (16)$$
$$f = \frac{1}{2\pi\sqrt{L_{cap}C}} \qquad (17)$$

, where L_{cap} is the internal stray inductance of each capacitor bank. Typically, both magnitude and frequency of the inrush current caused by back to back switching are very high compared to permissible values in the standards. Figure 9 shows the addition of an inrush reactor to each capacitor

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bank to limit the inrush current magnitude and frequency (and therefore I×f). With the addition of the inrush reactors, the inrush current magnitude, frequency, and "I×f" can be rewritten as in (18-20).

$$I_{peak} = \sqrt{\frac{2}{3}} \times \frac{n}{n+1} \times \sqrt{\frac{C}{L_{in}}} \times V_{LL} \qquad (18)$$

$$f = \frac{1}{2\pi\sqrt{L_{in}C}} \qquad (19)$$

$$I \times f = \sqrt{\frac{2}{3}} \times V_{LL} \times \frac{n}{n+1} \times \frac{1}{2\pi L_{in}} \qquad (20)$$

The required inrush inductance for each standard criterion can be calculated as follows.

- I×f requirement: $L_{in} = \frac{n}{n+1} \times \frac{V_{LL}}{\sqrt{6}\pi I \times f}$ (21)

,where I×f can be found from Table I for IEEE.

- I_{peak} requirement: $L_{in} = \frac{2}{3}C\left(\frac{V_{LL}}{I_{peak}}\right)^2\left(\frac{n}{n+1}\right)^2$ (22)

,where I_{peak} can be found from Table I for IEEE or section 2.1 for IEC.

- f requirement: $L_{in} = \frac{1}{4\pi^2 f^2 C}$ (23)

,where f can be found from section 2.1 for IEC.

Required L_{in}=MAX {(21), (22)} for IEEE and MAX {(22, 23)} for IEC   (24)

Figure 9. Application of inrush reactors to multiple capacitor banks.

4.2 Outrush current

Figure 10 shows a nearby breaker closing on to a fault, where inrush reactors are connected in series with each capacitor bank. Typically, the outrush current generated by multiple capacitor banks have high magnitude and frequency:

$$I_{peak} = \sqrt{\frac{2}{3}} \times V_{LL} \times (n+1) \times \sqrt{\frac{C}{L_{in}}} \qquad (25)$$

$$f = \frac{1}{2\pi\sqrt{L_{in}C}} \qquad (26)$$

An outrush reactor is added between the capacitor banks and the bus to limit the outrush current as shown in Figure 11. Below equations can be derived:

$$I_{outrush} = \sqrt{\frac{2}{3}} \times (n+1) \times \sqrt{\frac{C}{(n+1)L_{out}+L_{in}}} \times V_{LL} \qquad (27)$$

$$f = \frac{1}{2\pi\sqrt{(L_{in}+(n+1)L_{out})C}} \qquad (28)$$

$$I \times f = \sqrt{\frac{2}{3}} \times V_{LL} \times \frac{n+1}{2\pi(L_{in}+(n+1)L_{out})} \qquad (29)$$

The required outrush inductance can be calculated from below equations.

- I×f requirement: $L_{out} = \frac{V_{LL}}{\sqrt{6}\,\pi\,I.f} - \frac{L_{in}}{n+1}$ (30)

,where I×f can be found from section 2.2, IEEE-C0 breakers.

- I_{peak} requirement: $L_{out} = \frac{2}{3}C(n+1)\left(\frac{V_{LL}}{I_{peak}}\right)^2 - \frac{L_{in}}{n+1}$ (31)

,where I_{peak} can be found from section 2.1 (IEC) or 2.2 (IEEE) for C0 breakers.

- f requirement: $L_{out} = \frac{1}{(n+1)4\pi^2 f^2 C} - \frac{L_{in}}{n+1}$ (32)

,where f can be found from section 2.1 for IEC C0 breakers.

Required L_{out}=MAX {(30), (31)} for IEEE C0 or Max {(31), (32)} for IEC C0 beakers.   (33)
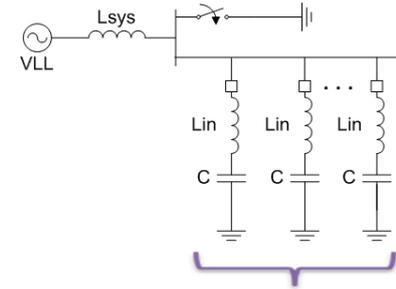

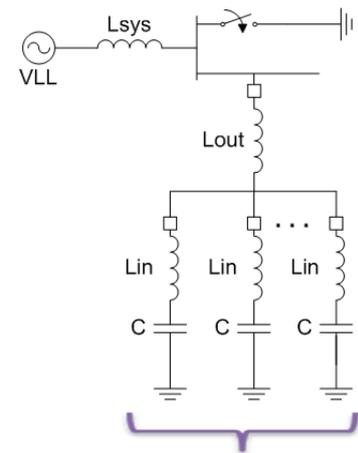Figure 10. Outrush current in multiple capacitor banks.

Figure 11. Addition of outrush reactor to multiple capacitor banks

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4.3 Inrush reactor current rating
4.3.1 Continuous current rating

The continuous current rating of inrush reactors can be calculated using (12-13) and Factors in Table II, where C is the rated capacitance of every individual capacitor branch in the bank.

4.3.2 Short time current rating

Figure 12 shows the worst case fault location for the inrush reactor. If the fault occurs at peak voltage, the discharge current from the capacitors will have maximum magnitude, and the DC component of the short circuit current from the system will be zero. On the other hand, if the fault occurs at zero voltage, there will be no discharge current from the capacitors, but the short circuit current from the system will have its maximum DC component as in (35). Assuming the fault occurs near peak voltage, and the damping factor of the high frequency circuit is relatively low, the peak current can be calculated as the short circuit current peak with zero DC value superimposed on the discharge current magnitude from "n" capacitor banks as (34).

$$I_{inrush,flt} \cong \left\{ \sqrt{\frac{2}{3}} \times \frac{n}{\sqrt{n+1}} \times \sqrt{\frac{C}{L_{in}}} \times V_{LL} \right\} + \left\{ \sqrt{2}I_{sc,rms} \right\}, \qquad (34)$$

where $\qquad I_{sc,rms} = \dfrac{V_{LL}}{\sqrt{3} \times 2\pi f_{sys}(L_{sys}+L_{out}+L_{in})} \qquad (35)$

$$I_{flt,peak} \leq 2\sqrt{2}I_{sc,rms} \qquad (36)$$

The rated mechanical peak current of the inrush reactor is the highest value of (34) and (36) as shown in (37), and the thermal short circuit current rating of the inrush reactor is as given in (35).

$$I_{L_{in},peak} = max\{I_{flt,peak} \ , \ I_{inrush,flt}\} \qquad (37)$$

n+1 already energized capacitors

Figure 12. Worst case fault location for inrush reactor.

4.4 Outrush reactor current rating
4.4.1 Continuous current rating

The continuous current rating of the capacitor bank is the product of the "Factor" from Table II and the rated bank current as calculated from (38), where $V_{cap,L-N}$ is the capacitor's rated phase voltage.

$$I_{continuous,out} = I_{bank} \times Factor, \ I_{bank} = 2\pi f_{sys}(n+1)CV_{cap,L-N} \qquad (38)$$
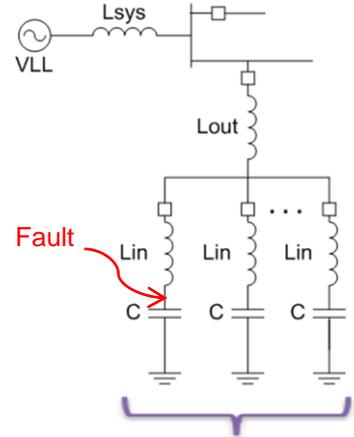
4.4.2 Short time current rating

There are two possible fault locations affecting the outrush reactor as shown in Figure 13. At Fault 1, the only transient current passing through the outrush reactor is the discharge current from the capacitor. The magnitude of this current can be calculated from (39). In case of Fault 2, the short circuit current from the system passes through the reactor, which can be calculated from (40). The highest of (39) and (40) is determined as the mechanical peak current rating of the reactor, and the thermal short circuit rating of the reactor can be calculated from (41).

At Fault 1: $I_{outrush} = \sqrt{\dfrac{2}{3}} \times (n+1) \times \sqrt{\dfrac{C}{(n+1)L_{out}+L_{in}}} \times V_{LL}$ (39)
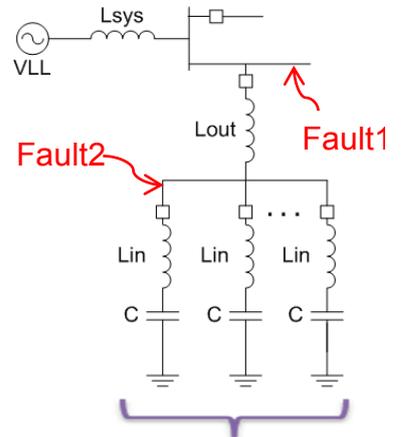
At Fault 2: $I_{flt,peak} \leq 2\sqrt{2}I_{sc,rms}$ (40)

$I_{sc,rms} = \dfrac{V_{LL}}{\sqrt{3} \times 2\pi f_{sys}(L_{sys}+L_{out})}$ (41)

$I_{L_{out},peak} = max\{I_{flt,peak} \ , \ I_{outrush}\}$ (42)

n+1 already energized capacitors

Figure 13. Possible fault locations affecting the outrush reactor.

5. EXAMPLE

Assume a 230 kV, 60 Hz system with equivalent inductance of 10 mH seen from the bus as shown in Figure 14. Three capacitor banks of 52.8 MVar each (C=2.65 μF) are connected to the bus through BRK1s (C1 circuit breakers rated at 245 kV, 2000 A, 40 kA); and there is a C0 BRK2 breaker near the bus. Assuming the stray inductance of each capacitor bank is 27 μH, the inrush current from back to back switching of the capacitors, and the outrush current through the close-on-to-fault BRK2 can be calculated as in Table III, assuming a total stray inductance of 60 μH between the banks and BRK2.

From Table III, both inrush and outrush currents exceed the standard limits, and therefore inrush reactors are needed to protect BRK1 and an outrush reactor is required to protect BRK2. Figure 15 (a) shows the PSCAD simulation results for inrush and outrush currents of the system in Figure 14. The simulation results yield current peaks and frequencies identical to calculated values given in Table III.

Table III. Inrush and outrush currents calculated for the example.

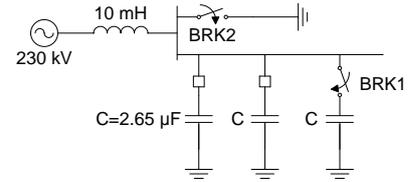|	$I{\times}f\,({\times}10^7)$	I_{peak} (kA)	f (kHz)
Inrush	78.6	41.8	18.8
Outrush	46.2	68	6.8
C0 BRK (IEEE)	2	50	N/A
C1 BRK (IEEE)	8.6	20	4.3

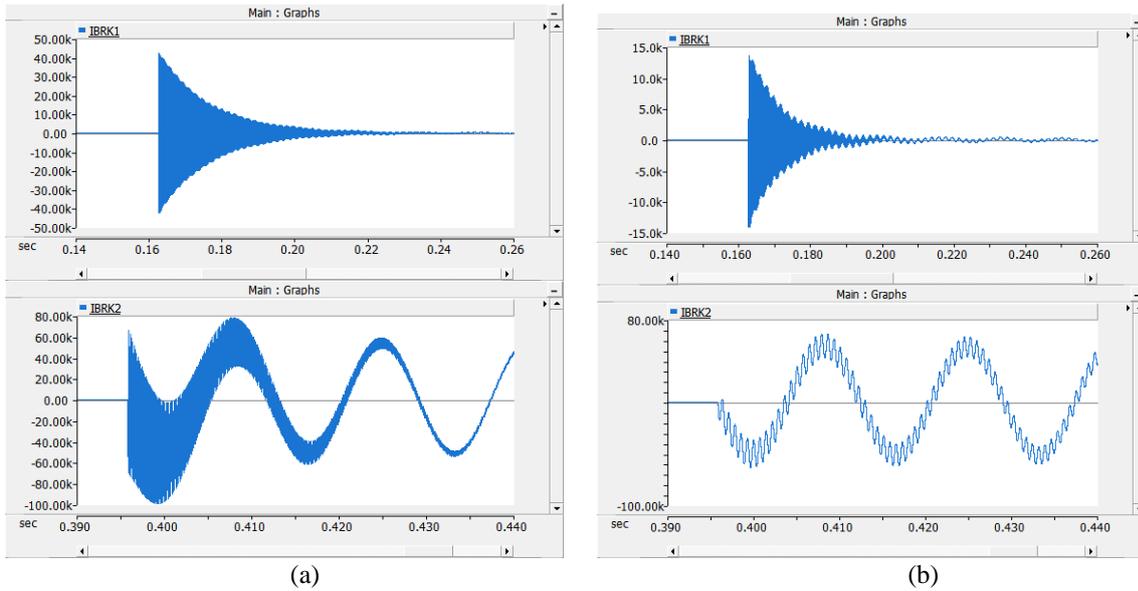Figure 14. Three 230 kV, 52.8 MVar capacitor banks.

(a)

(b)

Figure 15. PSCAD simulation results for inrush and outrush currents: (a) without inrush and outrush reactors, (b) with addition of inrush and outrush reactors.
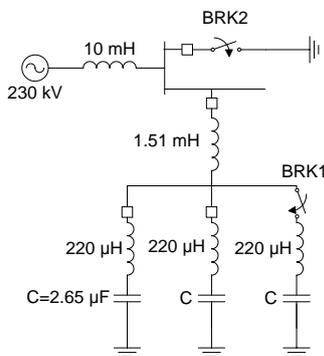

Figure 16. Example system with addition of inrush and outrush reactors.

Table IV. Inrush and outrush currents with the reactors in circuit.

	$I{\times}f\,({\times}10^7)$	I_{peak} (kA)	f (kHz)
Inrush	8.6	13.8	6.22
Outrush	2	14.1	1.4
C0 BRK (IEEE)	2	50	N/A
C1 BRK (IEEE)	8.6	20	4.3

Table V. Inrush and outrush Reactors current ratings specification.

Reactor type	Continuous current (A)	Thermal short circuit (kA) rms	Mechanical peak current (kA)	Discharge frequency (kHz)
Inrush	180	32	≤90[1]	6.22
Outrush	540	32.6	≤92	1.4

[1,2] The DC component and therefore the mechanical peak current from a short circuit depends on the circuit's damping ratio. The values given in this table assume zero damping.

From (24), the required total inrush inductance is found to be L_{in}=247 μH. Therefore, the required inductance of the inrush reactors in addition to the stray inductance of the capacitors is calculated to be 220 μH. From (33), the required inductance of the outrush reactor is found to be L_{out}=1.51 mH. Figure 16 shows the capacitor bank configuration with the addition of the inrush and outrush reactors. Table IV provides the calculated inrush and outrush currents with the addition of the reactors, and Figure 15 (b) presents the PSCAD simulation results for the inrush and outrush currents with the addition of the reactors. It can be found that the inrush and outrush reactors successfully limit the three parameters of I, f, and I×f below the standard limits and the PSCAD simulation results agree with the calculated quantities using the equations derived in this paper. Table V uses (12-13), (35), (37-38), and (41-42) and provides the proper sample current ratings for the inrush and outrush reactors required by the equipment manufacturer. It is important to note that inrush/outrush reactor design costs are often controlled by short circuit ratings. When specifying short circuit current duration, fault clearing time and maximum number of reclosing operations should be considered.

6. DISCUSSIONS

In this paper, the inrush reactors are added in series with every capacitor branch in multiple bank configurations. Optionally, one of the capacitor branches needs not be equipped with an inrush reactor, providing all other branches have one properly sized inrush reactor. Also, the inrush or outrush reactors can optionally be installed at the neutral side of the capacitor banks. This method has its advantages and disadvantages and should be chosen carefully. Also, in the application of series reactors, circuit breaker TRV considerations should be taken into account. Refer to [8] for details.

7. CONCLUSIONS

High magnitude and frequency of inrush current caused by the back to back switching of capacitor banks can cause damage to circuit breaker contacts, increase the probability prestrikes, and lead to over-voltages in CTs secondary circuits. Outrush currents with high magnitudes and frequencies also occur when a nearby breaker closes on to a fault, potentially causing damage to the breakers' contacts and also result in over-voltages in CTs secondary circuit. The paper derived and presented the mathematical formulae to calculate the required inductance for both inrush and outrush reactors, as well as the proper current rating specification for equipment manufacturers. The numerical calculations were validated by the PSCAD simulation results for a case study.

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