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Short Circuit Analysis of Power Systems with Inverter Interfaced Resources

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SUMMARY

Short circuit analysis is fundamental to design and protection of power systems, and the method of analysis is well established for power systems with conventional synchronous generators (SGs). However, the increasing penetration of inverter-interfaced resources (IIRs) which are electronically coupled to the grid alters the short circuit behavior of networks. This is due to the non-linear behavior of the power electronic converters which limit the short circuit currents just above the rated currents to protect the semiconductor devices in the converters. In the earlier period, IIRs were allowed to disconnect from the network during fault events due to their minor contribution to the recovery from disturbances compared to conventional generators. With increasing penetration, IIRs have a major impact on power system stability, and the system operators introduced a set of requirements through the grid codes to ensure a supporting action from IIRs, forcing them to remain connected during the faults. Thus, the contribution of IIRs to fault currents needs to be taken into account but modeling the non-linear behavior of an IIR during faults typically requires electromagnetic transient (EMT) simulation models. However, when performing a short circuit analysis during an early stage of planning or design process, a simple yet reasonably accurate methodology is required. Iterative short circuit analysis is an emerging method where the portion of the system with IIR is modeled as a voltage dependent equivalent source in a conventional short circuit program. The convergence and accuracy of these approaches are yet to be tested thoroughly.

In this study, a method for accurate calculation of short circuit currents in a power system with IIRs using phasor domain techniques is proposed. An iterative short circuit analysis algorithm is used to incorporate the non-linear behavior of the IIRs to get the correct phasor solution. The methodology employs a voltage dependent network equivalent (VDNE) to represent a subsystem with high penetration of IIRs in the phasor domain short circuit calculation process. The proposed VDNE framework utilizes a linear voltage source behind the Thévenin equivalent impedance to represent the conventional generators and a voltage dependent current source to capture the non-linear behavior of the IIRs. The VDNE parameters are derived by repeatedly simulating a detailed model of the portion of the network with IIRs in an EMT simulator, through an automated process. The results of the proposed methodology are validated by comparing with the fault current and voltages obtained from time domain simulations in PSCAD/EMTDC for three-phase to ground faults for IEEE 39 bus test system.

KEYWORDS

Inverter-interfaced resources, voltage dependent network equivalent, iterative short circuit analysis

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1 INTRODUCTION

The penetration of large-scale inverter-interfaced resources (IIRs) to transmission networks has been increasing recently. The IIRs such as solar PV, and Type III and Type IV wind turbine generators (WTGs) employ voltage source converters (VSCs) at the grid interface [1]. During a fault condition, power electronic converters inject controlled currents to the grid, typically limited around the rating of the converter to protect the semiconductor devices [2]-[3]. Moreover, the negative sequence components of the fault currents from the converters are eliminated or suppressed, and the fault current magnitude and the current response can depend on the voltage/frequency ride through functions. Therefore, the characteristics of the short circuit currents of power systems with IIRs differ from the fault currents observed in power systems with only conventional generation.

In a grid containing a high penetration of IIRs, time-domain (TD) simulations using electromagnetic transient (EMT) models are recommended for studies to validate protection and control designs, and it is the benchmark technique used in the power industry. The models and control algorithms of IIRs utilized for these studies are usually manufacturer specific, and often customized to a given site to meet the applicable grid code requirements. It is becoming a common practice for manufacturers to provide EMT models of IIRs with confidential control algorithms as black boxed EMT models to power utilities for use in design and protection studies. These models can accurately simulate the response of IIRs, for example, a fault in the transmission network.

However, repeated TD simulation of large transmission networks containing thousands of buses using EMT models is not practical for some types of studies such as short circuit analysis. TD fault analysis is a computationally demanding process which needs to simulate the system until settles at the pre-fault steady-state condition and then apply the fault and continue the simulation. This is highly time-consuming when electrical machines and prime movers such as wind turbines are modeled in the system. When performing a short circuit analysis during an early stage of planning or design process, a simple yet reasonably accurate methodology is desired.

Iterative short circuit analysis is emerging as a new technique where the portion of the system with IIR is modeled as a voltage dependent network equivalent (VDNE) source in a conventional short circuit program. Since the VDNE is non-linear, an iterative solution is required for the typically linear short circuit analysis [4]. The convergence and accuracy of these approaches are yet to be tested thoroughly. Most of the previous studies have been carried out utilizing a simplified Thévenin equivalent for the grid models [5],[6]-[7]. In [8], a phasor domain modeling approach for Type III WTG is discussed where the Type III WTG is represented by a controlled current source. An iterative solution approach is employed to account for the impact of the converter control actions. The model is limited to analyse three-phase balanced faults that occur in power systems. Reference [9] presents a steady-state modeling approach for Type IV WTG which is represented as a controlled current source. The converter control action is accounted through an iterative short circuit solution. The modeling approach presented in this study has the ability to represent a detailed EMT model in steady state. In addition, this model is able to account for different control schemes of Type IV WTG including fault ride through (FRT) control function and decoupled sequence control action.

This paper presents a partially automated method for accurate calculation of short circuit currents in a power system with IIRs using phasor domain techniques and utilizes a VDNE to represent a portion of the power system with IIR. VDNE parameters are obtained by repeatedly simulating a detailed model of the portion of the network with IIRs in PSCAD/EMTDC simulation software through an automated process. The automation allows convenient calculation of VDNE parameters for different cases, for example considering different pre-fault operating conditions of a wind power plant (WPP). An iterative short circuit analysis algorithm is used to compute fault currents in phasor domain, considering the non-linear VDNE behavior. The proposed VDNE based iterative short circuit analysis methodology is validated by comparing with the fault currents obtained from time-domain simulations in PSCAD/EMTDC for three-phase to ground faults for the IEEE 39-bus test system.

2 OVERVIEW OF IIR MODELING FOR ITERATIVE SHORT CIRCUIT ANALYSIS

In the proposed iterative short circuit analysis, the complete system is divided into two segments as depicted in Figure 1. The external system i.e., the large transmission network represented as a linear phasor-domain model, and the subsystem with IIR represented as a phasor domain non-linear model referred to as voltage dependent network equivalent (VDNE).

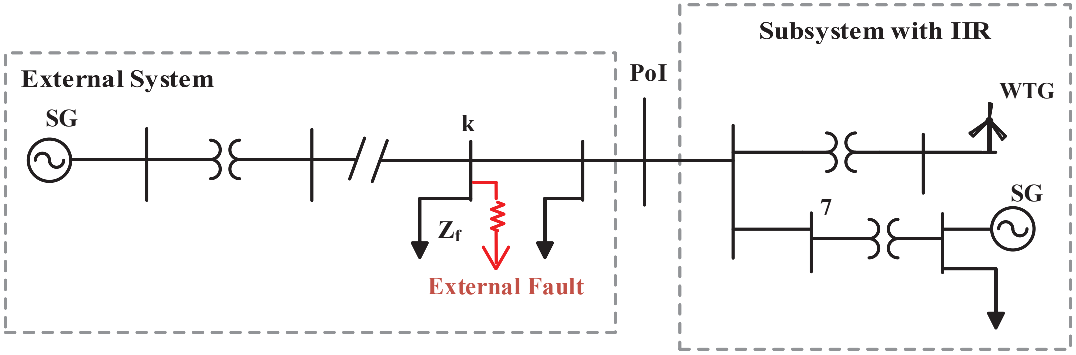
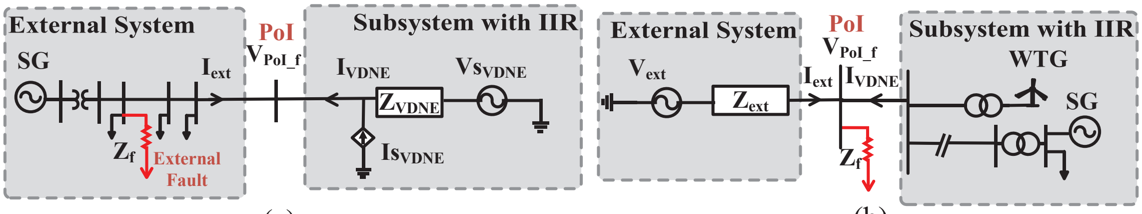


Figure 1 Division of a power system with IIR for iterative short circuit analysis

2.1 Voltage dependent network equivalent (VDNE)

The proposed iterative short circuit analysis runs the conventional phasor domain short circuit calculation process repeatedly to accommodate the non-linear fault current injections from the VDNE at the point of interconnection (PoI) for the faults inside the external system. Figure 2(a) shows the configuration of VDNE used to represent the subsystem consisting of the IIR in the bus impedance matrix-based iterative short circuit analysis. The proposed VDNE network consists of a voltage source (Vs_{VDNE}) behind the Thévenin equivalent impedance (Z_{VDNE}) and a voltage dependent current source (Is_{VDNE}) which represents the converter current injections. In Figure 2(a), V_{PoI_f} is the post-fault voltage at the PoI. I_{VDNE} is the current injected by VDNE at PoI, which is the addition of converter injected current Is_{VDNE} and the current contributed by the voltage source Vs_{VDNE}. The complex Thévenin impedance Z_{VDNE} represents the impedance of the subsystem as seen from the PoI, and includes the impedances of the synchronous generators, transformers, transmission lines, and loads in the subsystem with IIR, as well as the equivalent filter impedance of the IIR. Figure 2(b) represents the EMT simulation model used for the measurement-based approach to determine VDNE parameters.



(a) (b)

Figure 2 (a) VDNE for iterative short circuit analysis (b) EMT simulation model used for obtaining VDNE parameters

2.2 Finding the parameters of VDNE

In the VDNE model, the current contribution of the IIR is represented through Is_{VDNE}. This is a function of V_{PoI_f} and the calculation of Is_{VDNE} as a function of V_{PoI_f} is not straightforward. In order to obtain the parameters of the non-linear VDNE, detailed TD simulations are used and therefore, an EMT model of the subsystem with IIR is developed in PSCAD/EMTDC. During these TD simulations, the external system is represented as a Thévenin equivalent model with parameters V_{ext} and Z_{ext} as in Figure 2(b). These parameters can be easily determined from the short circuit capacity (MVA_F) and X/R ratio at the PoI.

The IIR can be a Type III or Type IV wind turbine generator, solar PV power plant, or battery energy storage system. This paper considers a wind farm consisting of Type IV WTGs with permanent magnet synchronous generators (PMSG) connected to the grid through back-to-back converters [10] as an example. In TD simulations, a wind farm is typically represented as an aggregated WTG model [11], but details such as the collector system can be modeled if necessary.

The VDNE parameters are derived by repeatedly simulating the detailed model of the subsystem with IIRs to achieve different voltages at PoI. The objective is to formulate a table of Is_{VDNE} versus V_{PoI_f} data by applying faults with varying fault impedances (Z_f) at the PoI. According to the equivalent circuit depicted in Figure 2(a), with the observed values of V_{PoI_f}, and $I_{VDNE,}$ the value of Is_{VDNE} can be computed. It is suggested that the data table comprises a series of V_{PoI_f} values varying from 0.1 pu to 1.0 pu with the steps of 0.05 pu. The value of the fault impedance Z_f required to obtain the desired voltage at the PoI is estimated as given in (1) and (2).

$$I_f = \frac{V_{ext} - n \times V_{step}}{Z_{ext}} \tag{1}$$

$$Z_f = \frac{n \times V_{step}}{V_{ext} - n \times V_{step}} \times Z_{ext} \tag{2}$$

where *n* is the number of fault voltage steps, I_f is the fault current and V_{step} is the minimum voltage step value.

Once the phasor values of the fault voltage and current are extracted from the time domain simulations (in this paper, FFT is used for this purpose), Is_{VDNE} is determined as,

$$Is_{VDNE} = I_f - I_{ext} - \frac{(Vs_{VDNE} - V_{PoI\_f})}{Z_{VDNE}} \tag{3}$$

The phasor value of Is_{VDNE} obtained through FFT has an arbitrary reference, and therefore not convenient to be used in the phasor domain analysis. In order to resolve this issue, the current, Is_{VDNE}, is resolved into two components, one in-phase with the PoI voltage, V_{PoI_f}, and the other in quadrature with V_{PoI_f} as shown in (4).

$$\begin{aligned} Is_{VDNE\ d} &= Is_{VDNE}\ \cos(\theta) \\ Is_{VDNE\ q} &= Is_{VDNE}\ \sin(\theta) \end{aligned} \tag{4}$$

$Is_{VDNE\ d}$ is the d component of the converter injected current, Is_{VDNE}, which is in phase with V_{PoI_f}, and $Is_{VDNE\ q}$ is the q component of the converter injected current, which is in quadrature to V_{PoI_f}. The angle θ is the phase angle difference between V_{PoI_f} and Is_{VDNE}. Finally, the data table will be generated by tabulating d and q components of Is_{VDNE} against $V_{PoI\_f.}$ The repeated simulation in PSCAD/EMTD is automated through Python programming language.

3 ITERATIVE SHORT CIRCUIT ANALYSIS METHODOLOGY

Once the VDNE parameters are obtained in a tabular format, the data can be utilized to analyze the faults in the external part of the network modeled in the phasor domain. Since the current injected by VDNE, I_{VDNE}, exhibits a non-linear behavior, an iterative short circuit solution approach is utilized.

Assume a three-phase fault occurs in bus k in the external grid. The initial fault current (I^0_F) and the fault voltage ($V^0_{F,k}$) for a fault at bus k are obtained by the classical short circuit calculation algorithm [12], ignoring the converter current injection Is_{VDNE}. Using the phasor domain equations, it is possible to compute the voltage at PoI. Next, the iterative short circuit calculation starts by calculating the initial steady-state current injection from VDNE, I^0_{VDNE}. The parameters of VDNE are available in the form of a table of converter currents injected to the interface bus at different PoI voltages during a fault as explained in Section 2.2. From this table, the total injected current from the VDNE (I^{iter}_{VDNE}) corresponding to the calculated fault voltage at the PoI at a given iteration number "iter" ($V^{iter}_{F,PoI}$) can be obtained. Consider that the injected current from the converter at the PoI is Is^{iter}_{VDNE} which consists of in-phase (d) and quadrature (q) injections. The total current injection from the VDNE at the PoI consisting of the converter current and the current contribution from Vs_{VDNE} is:

$$I^{iter}_{VDNE} = I^{iter}_{sVDNE} + \frac{Vs_{VDNE} - V^{iter}_{F,PoI}}{Z_{VDNE}} \tag{5}$$

Then the change in voltage at the faulted bus (bus k) due to the change in current injection at PoI (ΔI^{iter}_{VDNE}) can be calculated as $\Delta V^{iter}_{fVDNE,k}$.

$$\Delta V^{iter}_{fVDNE,k} = Z[k, PoI] \times \Delta I^{iter}_{VDNE} \tag{6}$$

Due to the deviation of faulted bus voltage, the change in fault current in the faulted bus becomes:

$$\Delta I_{F,k}^{iter} = \frac{\Delta V_{fVDNE,k}^{iter}}{Z[k,k] + Z_f} \tag{7}$$

As a result of the change in fault current, the bus voltages in the faulted system change. The corresponding bus voltage changes at PoI bus ($\Delta V_{fVDNE,PoI}^{\Delta,iter}$) can be computed, and PoI bus voltage can be updated as:

$$\Delta V_{f_{VDNE},PoI}^{\Delta,iter} = Z[PoI,k] \times (-\Delta I_{F,k}^{iter}) \tag{8}$$

$$V_{F,PoI}^{iter+1} = V_{F,PoI}^{iter} + \Delta V_{f_{VDNE,PoI}}^{\Delta,iter} \tag{9}$$

Then, the difference in $V^{iter}{}_{F,PoI}$ between consecutive iterations is obtained to evaluate the convergence criteria:

$$| V_{F,PoI}^{iter+1} - V_{F,PoI}^{iter} | < \varepsilon \tag{10}$$

The block diagram for the proposed iterative short circuit analysis is illustrated in Figure 3.

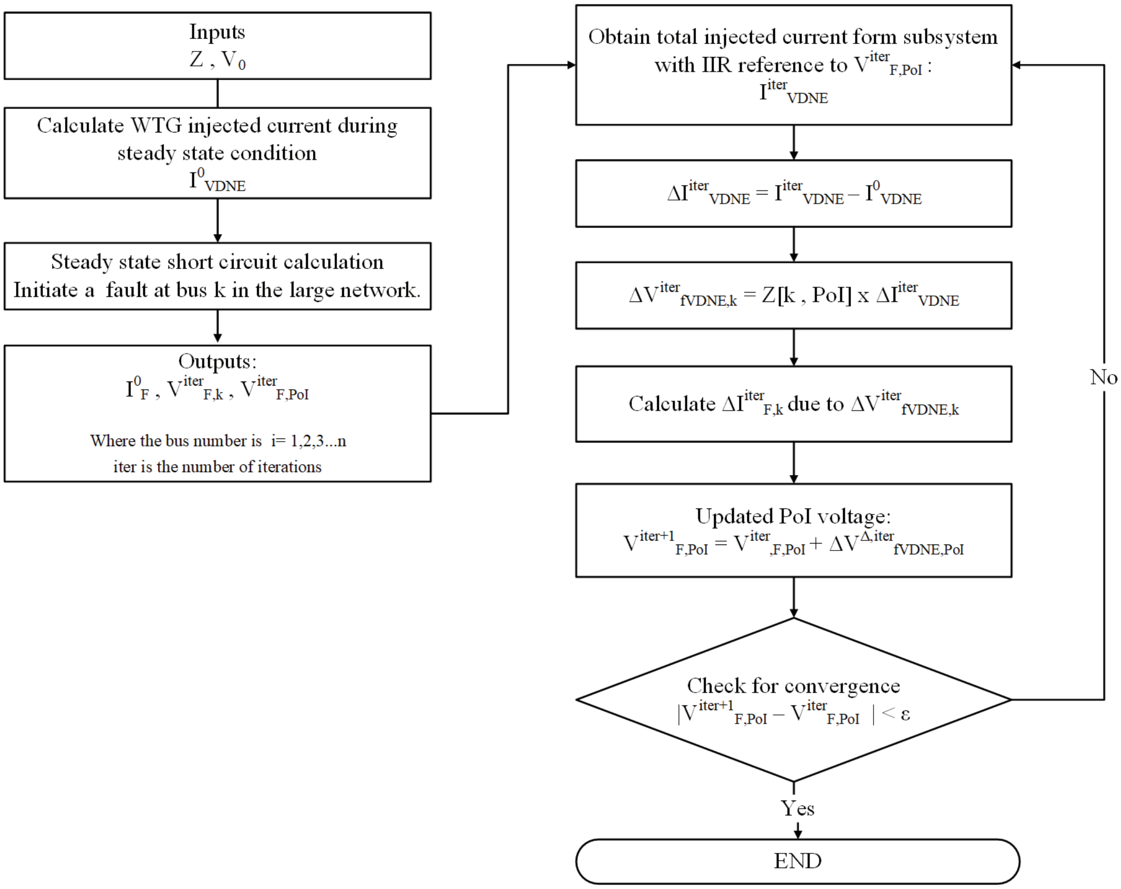


Figure 3 Iterative short circuit calculation process

4 SIMULATION EXAMPLE

The test system used for validating the proposed method is composed of 39 buses with a subsystem that includes a WPP connected at Bus 39. Bus 37 is the slack bus. The WPP is represented using an aggregated model of 150 Type IV WTGs, each with 2 MW active power rating. The schematic diagram of the IEEE 39-bus test system with the added WPP is illustrated in Figure 4. The data for the IEEE 39 bus system can be found in [13]. A power flow analysis was run to establish the pre-fault voltages at all buses including at PoI.

The input parameters to pertaining to the external system for performing VDNE parameter calculation in PSCAD/EMTDC environment are as follows. The pre-fault bus voltage at PoI, V^0_{PoI}, is $1.0 \angle 0.0^{\circ}$. The fault MVA at the PoI bus is 2661.09 MVA and the X/R ratio of the PoI is 4.749.

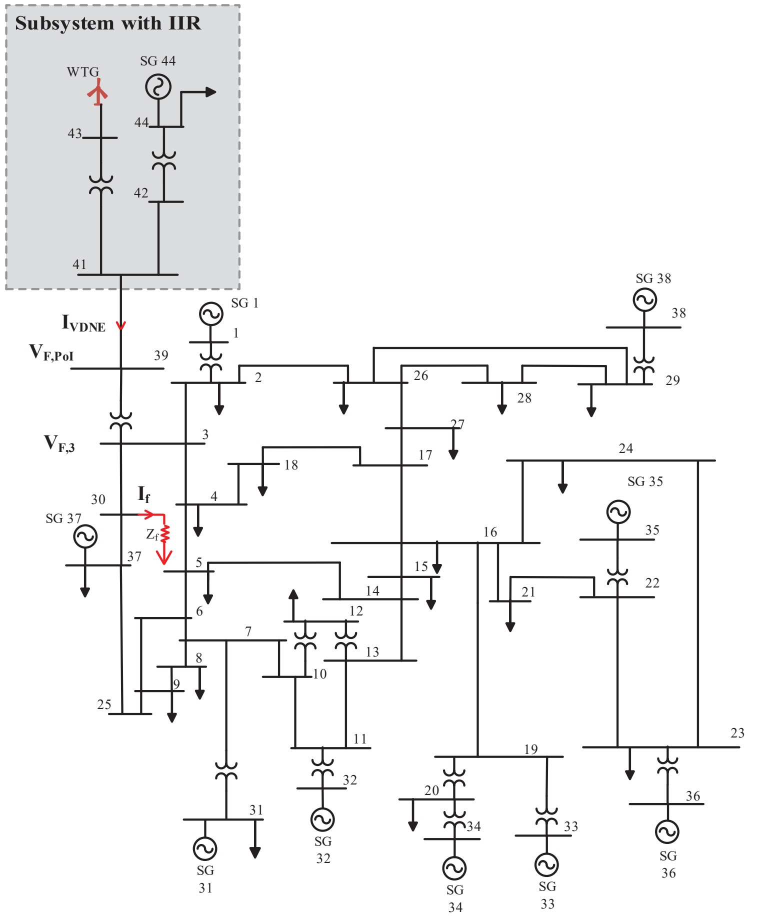
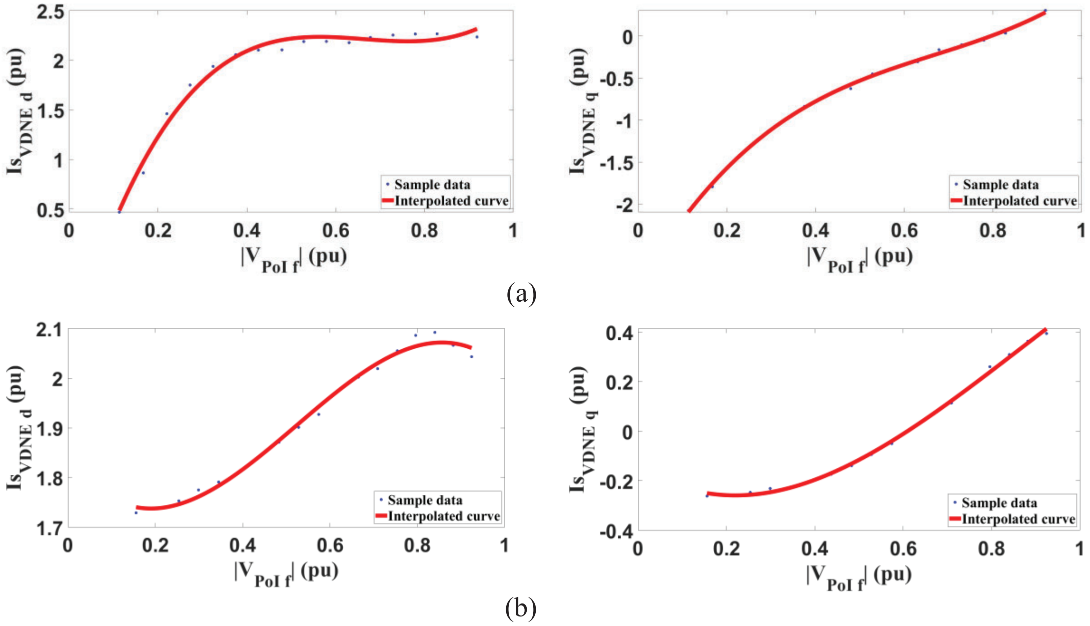


Figure 4 IEEE 39-bus test system augmented with a wind power plant

Sample sets of converter injected currents $Is_{VDNE\ d}$ and $Is_{VDNE\ q}$ measured 3-cycles and 6-cycles after fault inception are tabulated at nominal wind speed which is 10 km/h. Two instances after the fault inception are considered to illustrate that the fault current injections from the converters vary with time, depending on the operating mode and the activation of the voltage ride through function. The variations of $Is_{VDNE\ d}$ and $Is_{VDNE\ q}$ of the WPP with the fault voltage at the PoI are depicted in Figure 5(a) and Figure 5(b) for the measurements taken 3-cycles and 6-cycles after the fault inception respectively. The third-degree polynomial fitted the data with a 95% confidence bound is also shown on the same plots.

Once all the parameters of the VDNE of the 39-bus test system are identified, the iterative short circuit analysis is performed for a three-phase-to-ground fault applied at Bus 30, a location outside the part of the network modeled in VDNE. The fault resistance is varied, and the calculations are made 3 and 6-cycles after the inception of the fault.

The results are compared with fault analysis results obtained by simulating the complete power system including the WPP in PSCAD/EMTD for verifying the accuracy. The computed fault voltages and currents, and the current and voltage at the PoI during the three-phase to ground fault at Bus 30 are shown in Table 1. The voltage and current values are given in pu. When compared with the EMT solutions, the fault current and voltage values obtained from phasor domain computations using the iterative method were very close; the highest percentage error remained below 2.5%.



(a)

(b)

Figure 5 Variations of $Is_{VDNE\ d}$ and $Is_{VDNE\ q}$ (in pu) with the voltage magnitude at the PoI during three-phase faults (a) after 3 cycles (b) after 6 cycles

Table 1 Comparison between phasor domain and EMT solution

Fault Resistance	Parameter	Phasor Domain Solution	EMT solution	Magnitude error %
3 cycles after the inception of the fault				
R_f= 0	$V_{F,PoI}$	0.918 ∠ -33.97 °	0.917 ∠ -33.60 °	0.1
	$V_{F,3}$	0	0	0.0
	I_F	6.150 ∠ -97.37 °	6.074 ∠ -97.21 °	1.3
	I_{VDNE}	2.26 ∠ -46.68 °	2.29 ∠ -32.95 °	1.4
R_f=10	$V_{F,PoI}$	0.920 ∠ -34.62 °	0.921 ∠ -34.22 °	0.1
	$V_{F,3}$	0.112 ∠ -91.81 °	0.11 ∠ -91.53 °	1.8
	I_F	5.950 ∠ -92.18 °	5.838 ∠ -91.53 °	1.9
	I_{VDNE}	2.260 ∠ -47.47 °	2.273 ∠ -34.1 °	0.6
R_f=20	$V_{F,PoI}$	0.929 ∠ -35.15 °	0.927 ∠ -34.72 °	0.2
	$V_{F,3}$	0.215 ∠ -86.93 °	0.211 ∠ -86.33 °	1.9
	I_F	5.69 ∠ -87.05 °	5.569 ∠ -86.33 °	2.2
	I_{VDNE}	2.260 ∠ -47.75 °	2.261 ∠ -34.91 °	0.01
6 cycles after the inception of the fault				
R_f=0	$V_{F,PoI}$	0.920 ∠ -34.29 °	0.909 ∠ -33.75 °	1.2
	$V_{F,3}$	0	0	0.0
	I_F	6.03 ∠ -98.54 °	6.011 ∠ -97.21 °	0.3
	I_{VDNE}	2.117 ∠ -52.22 °	2.116 ∠ -25.68 °	0.05
R_f=10	$V_{F,PoI}$	0.927 ∠ -34.92 °	0.914 ∠ -34.35 °	1.4
	$V_{F,3}$	0.110 ∠ -92.78 °	0.109 ∠ -91.51 °	0.9
	I_F	5.890 ∠ -92.78 °	5.778 ∠ -91.51 °	1.9
	I_{VDNE}	2.105 ∠ -51.42 °	2.108 ∠ -26.75 °	0.2
R_f=20	$V_{F,PoI}$	0.930 ∠ -35.39 °	0.920 ∠ -34.84 °	1.1
	$V_{F,3}$	0.251 ∠ -87.39 °	0.208 ∠ -86.28 °	0.9
	I_F	5.61 ∠ -87.39 °	5.513 ∠ -86.28 °	1.7
	I_{VDNE}	2.110 ∠ -51.09 °	2.106 ∠ -27.49 °	0.2

5 CONCLUSIONS

This paper presented a mathematical framework and an automated process to obtain a voltage dependent network equivalent to represent a subsystem with IIR, (Type IV WTGs used as an example) for short circuit analysis. The proposed VDNE framework utilizes a voltage dependent current source to capture the non-linear behavior of the IIRs. The VDNE parameters were derived by repeatedly simulating a detailed model of the WPP and an equivalent of the external network in PSCAD/EMTDC through an automated process.

An iterative short circuit analysis algorithm was presented to incorporate the non-linear behavior of the IIRs to get the correct phasor solution. The proposed VDNE based iterative short circuit analysis methodology was tested by simulating a three-phase to ground faults on the IEEE 39-bus test system. The fault calculation was carried out by varying the fault impedance for two different time points after the fault inception. The phasor solution obtained by the proposed model was proven accurate in comparison to the time-domain simulation results.

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